

# Expanding the Voltage Range of the HIP1020 FET Driver

**Application Note** 

September 27, 2006

AN1263.0

Authors: David Laing and Trevor Earle

The HIP1020 is a flexible FET driver designed to support up to 12V and down to 3.3V supplies. Yet, using a simple network, you can expand the FET driver's voltage range. This Application Note will offer a solution for controlling 24V, 5V and -5V supplies. We used the HIP1020 but the concepts can be applied to many FET controllers of this type.

The solution is divided into three FET designs, first starting with the simple +5V controller, then addressing the +24V controller and finishing up with the -5V controller. We will address most of the common MOSFET types and discuss why each MOSFET was selected for the particular supply voltage.

Input and Output requirements:

 $V_{IN} = 24V$ 

V<sub>SFO1</sub> = +24V @1A

V<sub>SEQ2</sub> = +5V @2A

V<sub>SFO3</sub> = -5V @1A

Before we start, a quick review of how the HIP1020 operates with  $V_{CC}$  = 12V is in order. The HIP1020 applies a linear ramp voltage to the Gate of the MOSFET controlling the 3.3V, 5V and 12V power supplies. The internal charge pump doubles a 12V bias to deliver the high-side drive capability (HGATE) required when using more cost-effective N-Channel MOSFETs. The charge pump ramps the voltage on HGATE from 0V to 22V in about 4ms. This allows either a standard or a logic-level MOSFET to become fully enhanced when used as a high-side switch for 12V power control. The voltage on LGATE ramps from 0V to 16V allowing the simultaneous control of 3.3V and/or 5V MOSFETs. Here lies the problem, how to control +24V and -5V when the HIP1020 is not capable of driving the MOSFETs to support such a requirement.

NOTE: This application uses FET as switches. To prevent damage to the FETs, they must operate either in full conduction (minimum RDS(ON)) or completely off and not in the linear region. When the FET is on, there is minimum RDS(ON) and minimum voltage difference between the Source terminal and Drain terminal. This minimizes the power losses (heat) due to I<sup>2</sup>R losses. We use the term "on", in relationship to the FET's state, to imply the FET is in full conductions and not in the linear region.

We need to first address powering the HIP1020 with 24V when the V $_{CC}$  Max = 14.5V. The operating conditions for the HIP1020 V $_{CC}$ , is 12V ±10%. Yet all we have is 24V supply. We need to design a simple low cost 12V supply for the HIP1020.

First, you need to understand the HIP1020 supply requirement. From the data sheet,  $V_{CC}$  = 12V will draw a maximum of 2.3mA. This establishes the basis for the power requirement of the 12V supply, which is just under 30mW to power the HIP1020.

### HIP1020 Power Supply (Figure 1)

A simple and low-cost solution we recommend is a Zener Diode type supply. The HIP1020 is specified to operate with 12V ±10% supply and still meet the data sheet specification. Computing the Zener biasing resistor requires we determine the voltage drop and the total current through the resistor.

Since we are designing a 12V supply, the voltage drop is:

$$V_{RZENER} = V_{CC} - V_{ZENER} = 24V - 12V = 12V$$
 (EQ. 1)

Current through the Zener bias resistor would be the sum of the  $I_{CC}$  of the HIP1020 and the Zener reverse bias current. We selected a nominal 2mA reverse Zener current based on a typical 1/4 watt Zener diode. (Zener wattage would be  $(12V \times 2mA) = 24mW$ , well within the Zener rating).

$$I_{RZENER} = I_{HIP1020} + I_{zenerbias} = 2.3mA + 2mA = 4.3mA$$
 (EQ. 2)

$$R_{ZENER} = 12V/4.3mA = 2.79k\Omega$$
 (EQ. 3)

To keep the cost down, we used a low cost 2.7k resistor, as the Zener bias current limiting resistor value is not critical to the operation. The HIP1020 and the Zener would draw about 4.3mA max or about 50mW total, well within a 1/4 watt Zener resistor power requirement. You might consider using a three-tab regulator, but that would add cost and board space over a single resistor and 1/4 watt Zener diode.

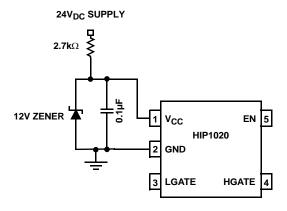


FIGURE 1. ZENER POWER SUPPLY

#### **Application Note 1263**

You can find additional tutorials on the web to better understand Zener diode operation and supply design, such as: http://www.allaboutcircuits.com/vol\_3/chpt\_3/9.html

Why need a Zener charging cap? During operation there are Gate-Source charge current requirements due to the Gate-Source capacitance. To meet the local current needed for charging the Gate-Source capacitance, the rule of thumb is the local V<sub>CC</sub> supply capacitor should be 10 times that of the Gate-Source capacitance to supply the needed Gate charging surge current for turning on the N-Channel MOSFET.

A typical application for the HIP1020 would be driving two power N-MOSFETs. Their combined Gate capacitance, CISS, is in the region of 1000pf. Turning on these N-MOSFETs will require a reasonable turn-on/surge current from the HIP1020 supply. A good rule of thumb is to have the local bypass capacitance about ten times that of the combined Gate capacitance to handle the turn-on currents. A low-cost ceramic 0.1µF capacitor would support this requirement. This design will not need as large a value capacitor, but you do need to consider the turn-on currents in determining the local bypass capacitance value.

We now have the power supply for the HIP1020, let us start into the circuit design for the +5V supply controller. Borrowing from the data sheet FN4601, page 1, figure 1, V5 in and V5 out, turning on the +5V MOSFET is straight forward but it is good to review a few basic power MOSFET rules of thumb.

#### Basic Rules of Thumb for Enhanced Power **MOSFETs**

N-Channel MOSFET — V<sub>GS</sub> should be between 5V and 10V or greater to drive the MOSFET to fully enhanced operation or heavy conduction to reduce the R<sub>DS(on)</sub>, depending on the type N-Channel MOSFET. But do not forget about the body diode in the N-Channel power MOSFET that is essentially a large diode with its cathode tied to the Drain and anode to the Source.

P-Channel MOSFET — VGS should be between -5V and -10V or less to drive the MOSFET to fully enhanced operation or heavy conduction to reduce the R<sub>DS(on)</sub>, depending on the type P-Channel MOSFET. Again, do not forget about the body diode in the P-Channel power MOSFET that is essentially a large diode with its anode to the Drain and cathode to the Source.

Selecting MOSFETs — you need to consider at least seven key parameters before making your initial selections:

MOSFET type (N-Channel or P-Channel),

Type - Logic Level or Standard

Operating voltage V<sub>DS</sub>,

Current requirement/Rds(on),

Power dissipation

**Body Diode Presence** 

VGS maximum

MOSFET suppliers offer parametric selection tables to assist you in choosing the correct MOSFETS.

Hereinafter, N-Channel MOSFET will be referred to as the N-MOSFET and the P-Channel MOSFET will be referred to as the P-MOSFET.

### Designing the +5V Controller (Figure 2)

The HIP1020 pin 3 'LGATE' will drive the Gate of the +5V supply (V<sub>5</sub> and V<sub>5OUT)</sub> N-MOSFET to about 16V above ground, well above a desired V<sub>GS</sub>. At the start, the Source is connected to the load but the N-MOSFET is not yet turned on. So, VGS will be equal to the voltage at pin 3, LGATE to ground. As the Gate voltage raises to 16V, the MOSFET will start to turn on and conduct, lowering the Gate to Source voltage, VGS. At full conduction, VGS will reach about 11V as the Source reaches +5V. At this point, V<sub>GS</sub> is still sufficient for the N-MOSFET to be in full conduction with the minimum  $R_{DS(on)}$ .

NOTE: The +5V supply is connected to the Drain to prevent the body diode from being forward biased.

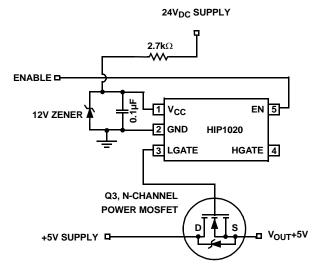


FIGURE 2. +5V N-MOSFET DRIVER

### Designing the +24V Controller (Figure 3)

The problem is: how to control the 24V supply when the HGATE, pin 4, only charge pumps up to 22V when  $V_{CC}$  = 12V? This 22V is well below the necessary Gate drive voltage needed for the N-MOSFET, with its Drain tied to 24V, to switch on the 24V. The maximum supply we could expect for a standard N-MOSFET to control would be in the range of 12V to 17V where: fully enhanced FET  $V_{GS}$  is between 5V, for a logic level N-MOSFET and 10V for a standard power N-MOSFET.

Raising V<sub>CC</sub> for the HIP1020 is limited to the absolute maximum V<sub>CC</sub> of 14.5V. Thus, even if we attempted to raise V<sub>CC</sub> in order to increase the charge pump output voltage, we cannot reach the V<sub>CC</sub> level necessary to generate the V<sub>GS</sub> needed to turn on the N-MOSFET.

So, we need to look at using a P-MOSFET. Turning on the channel, the Gate of the P-MOSFET needs to be below the Source by the same 10V or more. Thus, if we connect the Source to 24V and pull down the Gate, we will turn on the P-MOSFET, and pulling the Gate near the Source, will turn the P-MOSFET off.

If we just replaced the N-MOSFET with the P-MOSFET and tie Source to 24V and the Drain to the output, the P-MOSFET logic will be opposite of the N-MOSFET. In this configuration you will not be able to turn off the P-MOSFET. HGATE going high, 22V,  $\rm V_{GS}$  of the P-MOSFET will never reach the full pinch off level. Note that P-MOSFET  $\rm V_{GS}$  need to reach near 0V to turn off the P-MOSFET. HGATE going low will exceed the maximum  $\rm V_{GS}$ .

The HIP1020 HGATE output logic needs to be inverted to make use of the P-MOSFET. We can accomplish the inversion using a N-MOSFET as a switch in series with the

P-MOSFET Gate. Now with the N-MOSFET Drain in series with the P-MOSFET Gate and a resistor between the P-MOSFET Source and Gate, when the N-MOSFET turns off (HGATE goes low), the resistor will pull up the P-MOSFET Gate to the Source. This action will turn off the P-MOSFET. Turning on the P-MOSFET will require the Gate to be pulled down to about 10V or more

To turn on the P-MOSFET, a simple 2:1 voltage divider will drive the Gate near 12V below the Source. If we connect a resistor from the Source to ground of this N-MOSFET, when HGATE is high, the N-MOSFET is on, pulling down the P-MOSFET Gate and turning on the 24V supply.

Figure 3 circuit functions as follows. The N-MOSFET and two resistors form an inverting circuit and a 2:1 voltage divider. When HGATE is low, the N-MOSFET will turn off. The resistor between the P-MOSFET's Source (24V<sub>DC</sub> supply) and Gate will pull the Gate to the Source, turning off the P-MOSFET. HGATE high will turn on the N-MOSFET and the resistor divider will pull the P-MOSFET Gate towards ground, in this case 12V, and forces the P-MOSFET into heavy conduction. Keep in mind we cannot exceed the maximum P-MOSFET and N-MOSFET terminal voltages, especially V<sub>GS</sub> (typically 20V for most standard power MOSFETs)

The only issue remaining is selecting the series voltage divider resistors. The upper limit of the upper resistor network is set by the Gate leakage current and the maximum turn-off time (RC where C is the Gate capacitance of the P-MOSFET). The lower limit of the resistor's network is limited by how little current is to be drawn from the +24V supply. The mid-point voltage is limited to the maximum  $V_{\mbox{\footnotesize{GS}}}$  of the P-MOSFET and the turn-on time requirements. We selected two series  $10\mbox{k}\Omega$  resistors. .

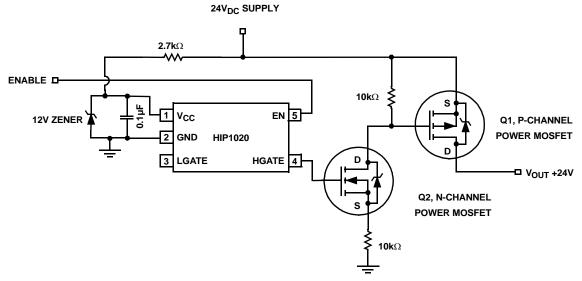


FIGURE 3. CONTROLLING THE +24V SUPPLY

The  $10k\Omega$  series network will, when HGATE is low (OFF), pull the P-MOSFET Gate to +24V and thus turn off the +24V supply. Conversely, when HGATE is high (ON), the N-MOSFET is on and the P-MOSFET gate is pulled to mid-range, or about 12V, by the series voltage divider resistors. The supply current draw would be 1.2mA when the +24V supply is on. Since we selected two  $10k\Omega$  resistors, the turn-off/on time would be the same or about 75µs (RC =  $10k\Omega$  and  $C_G$  = 1000pF) or about three time constants. The divider will place 12V on the P-MOSFET Gate,  $V_{GS}$ , and is well within the acceptable range for the maximum  $V_{GS}$ .

### Designing the -5V Controller (Figure 4)

You might consider using a simple N-MOSFET switch as we did the +5V supplies, but there are a few issues to consider: how to turn off the N-MOSFET and how to turn on the N-MOSFET without exceeding  $V_{\mbox{GS}}$  max. The following sections discuss these issues.

#### How to Turn Off the N-MOSFET

Turning off the -5V supply N-MOSFET is similar to how we turned off P-MOSFET of the +24V supply. But first the

design must take into consideration the -5V N-MOSFET switch body diode. The Source will have to be connected to the -5V supply to ensure back biasing of its body diode. Turning off the N-MOSFET will require the Gate to be pulled down to the Source. This can be done using, as we did with the +24V supply, a  $10k\Omega$  between the Gate and Source.

## How to Turn On the -5V N-MOSFET without Exceeding V<sub>GS</sub> Maximum

Turning on the -5V N-MOSFET controller will be more difficult.

You might consider using LGATE to direct drive the controller. But here again, using LGATE (High/ON is typically +16V) to drive the Gate would exceed the maximum  $V_{GS}$  (16V - (-5V) = 21V).

You might consider the approach we took for the +24V controller, using a voltage divider to reduce  $V_{GS}$  to within safe limits. But LGATE has limited driver current and cannot adequately drive more that 10µA. Using a resistive voltage divider would load down LGATE and adversely impact the voltage ramp to the +5V N-MOSFET Gate.

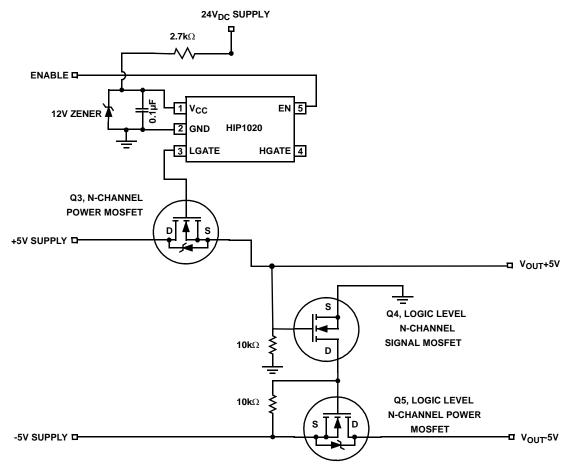


FIGURE 4. -5V CONTROLLER

#### Application Note 1263

Another point to consider would be using LGATE to directly drive both the +5V controlling N-MOSFET and the -5V controlling N-MOSFET. Yet, when LGATE's output is low or ground, this circuit forms a series voltage divider between ground and the -5V Source. When LGATE goes low, the controlling N-MOSFET Gate will be at some level below ground but not to the needed -5V to turn off the -5V supply.

We chose to use the +5V supply output as the controller for the -5V controller. The +5V supply output will overcome two limitations: LGATE current limitation and  $V_{GS}$  limitations.

One additional benefit is that using the +5V output will allow us to ramp the -5V supply as the +5V supply ramps.

The +5V supply output can certainly drive a small additional load. Connecting the +5V output to the -5V N-MOSFET Gate would place +5V on the Gate and with -5V on the Source of the -5V controller. Now  $V_{GS}$  will not exceed 10V.

But this configuration would not turn off the -5V controller. Don't forget if the +5V supply load is present, it would appear as a small resistor,  $5\Omega$  (5V/1A =  $5\Omega$ ). This resistor network would be, ground through the load to the -5V N-MOSFET Gate, through the  $10k\Omega$  to the Source at -5V. To turn off the -5V N-MOSFET, in this configuration, you would need to use a sub-one- $\Omega$  Gate-to-Source resistor to pull the Gate very close to the Source. This sub-one- $\Omega$  will, in turn, overload the +5V and -5V Source supplies as it will be a sub-one- $\Omega$  load across -5V Source to +5V output.

A plausible solution would be to use the +5V supply output to control an N-MOSFET/switch. This switch would also help to isolate the -5V Source from the +5V load. The switch would connect ground onto the -5V N-MOSFET Gate and turn on

the -5V supply when the +5V supply is on. When the +5V supply turned off, the -5V supply would then turn off by having a  $10k\Omega$  resistor between its N-MOSFET Gate and Source.

Selecting the N-MOSFET switch, we have two issues to consider: The maximum  $V_{GS}$  is =5V and the body diode must not be present. The switch's Gate will be controlled by 0V to +5V, far from the +10V needed to turn on a standard N-MOSFET. Logic level N-MOSFETs will turn on with VGS=5V. If there were a body diode present, the diode would be forward biased when the N-MOSFET is on or off, thus not shutting off the -5V N-MOSFET controller. So, using a small signal logic level N-MOSFET would act as the required switch and not have a body diode.

The -5V N-MOSFET has the same issue of maximum  $V_{GS}=5V$ , but we are not concerned about the body diode in this case. Thus, a logic level power N-MOSFET would work well in this application as shown in Figure 4. Turning off the logic level N-MOSFET would be the same as before, a simple  $10k\Omega$  resistor Gate to Source would turn off the logic level N-MOSFET when the +5V supply is off.

### Summary

Understanding the different types of MOSFET and their characteristics, you can expand the capabilities of many MOSFET drivers beyond their design limitations. Please remember, even though we focused on HIP1020, the basics of this application note can be applied to many MOSFET drivers of similar functionality. By adding two MOSFETs and a few resistors, we have extended the MOSFET driver's voltage range. See Figure 5.

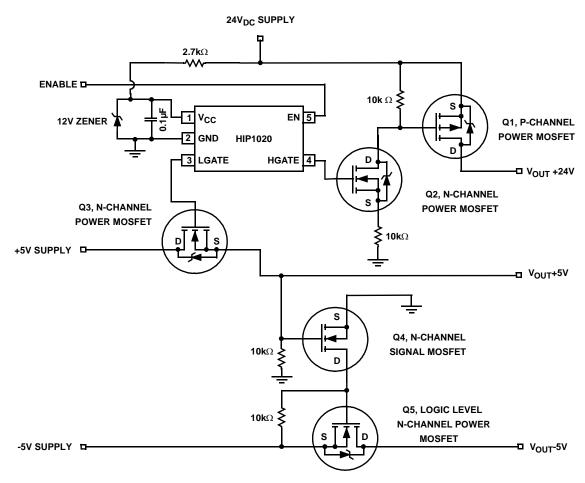


FIGURE 5. COMPLETED POWER SUPPLY CONTROLLER DESIGN

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.